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167	7590 07/21/2004			EXAMINER		
		JAWORSKI L L P	HENN, TIMOTHY J			
PATENT DOCKETING 29TH FLOOR 865 SOUTH FIGUEROA STREET				ART UNIT	PAPER NUMBER	
LOS ANGE	LES, CA	900172576		2612		
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Please find below and/or attached an Office communication concerning this application or proceeding.

•		Application	n No.	Applicant(s)					
		09/497,05	1	LEE ET AL.					
	Office Action Summary	Examiner		Art Unit					
		Timothy J	Henn	2612					
Period fo	The MAILING DATE of this communication or Reply	appears on the	cover sheet with the c	orrespondence ad	dress				
THE I - Exter after - If the - If NO - Failu Any r	ORTENED STATUTORY PERIOD FOR REMAILING DATE OF THIS COMMUNICATIOnsions of time may be available under the provisions of 37 CFR SIX (6) MONTHS from the mailing date of this communication. period for reply specified above is less than thirty (30) days, a period for reply is specified above, the maximum statutory per to reply within the set or extended period for reply will, by stately received by the Office later than three months after the med patent term adjustment. See 37 CFR 1.704(b).	N. R 1.136(a). In no eve reply within the statu riod will apply and wil atute, cause the appli	nt, however, may a reply be tim tory minimum of thirty (30) day: expire SIX (6) MONTHS from cation to become ABANDONE	nely filed s will be considered timel the mailing date of this co D (35 U.S.C. § 133).					
Status									
1)⊠	Responsive to communication(s) filed on 20	6 April 2004.							
·									
′=	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
5)□ 6)⊠ 7)⊠	, , , , =								
Applicati	on Papers								
9)□	The specification is objected to by the Exam	niner.							
10)⊠	The drawing(s) filed on <u>26 April 2004</u> is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
11)	Replacement drawing sheet(s) including the cor The oath or declaration is objected to by the	· ·							
Priority u	ınder 35 U.S.C. § 119								
12) a)[Acknowledgment is made of a claim for fore All b) Some * c) None of: 1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the papplication from the International Bur See the attached detailed Office action for a	ents have been ents have been priority docume reau (PCT Rule	n received. n received in Applicati nts have been receive e 17.2(a)).	on No ed in this National	Stage				
Attachmen	t(s)								
	e of References Cited (PTO-892)		4) Interview Summary Paper No(s)/Mail Da						
3) Inform	e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB r No(s)/Mail Date		5) Notice of Informal F 6) Other:		O-152)				

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DETAILED ACTION

Drawings

1. The drawings were received on April 30, 2004. These drawings are accepted, accordingly the drawing objections in the previous office action are withdrawn.

Specification

2. The amendment filed on April 26, 2004 overcomes the objections to the specification, these objections are therefore withdrawn.

Claim Objections

3. The amendment filed on April 26, 2004 overcomes the objections to claims 2, 5 and 6, these objections are therefore withdrawn.

Response to Arguments

4. Applicant's arguments filed April 26, 2004 in paper number 5 have been fully considered but they are not persuasive.

In the amendment the applicant argues that Mimura teaches an effective readout of a "zig-zag" pattern for both the even and odd fields as shown in figure 2(a). While this is undoubtedly the case, it is noted that claim 1, as is currently written, does not require a zig-zag readout pattern for only one field. Claim 1 recites "characterized in that said first and second light detecting elements in each row are alternately disposed

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and activated by first read lines to generate odd field signals, and in that said first and second light detecting elements in two adjacent rows disposed in a serrated manner are activated by second read lines to generate even field signals". In the interpretation used in the rejection of claim 1, the first elements correspond to the elements of the first row of Mimura and the second elements correspond to the elements in the second row of Mimura. As can be seen from figure 2(a), the first elements (i.e. first row; R-B-G pixels) and the second elements (i.e. second row; G-R pixels) are alternately disposed (i.e. row 1 - row 2 - row 1 - row 2) and are activated by first read lines (i.e. the first zig-zag readout pattern) to generate odd field signals and that first and second light detecting elements in two adjacent rows (i.e. row 2 and row 3) are disposed in a serrated manner (see figure 2(a)) and are activated by second read lines to generate even field signals (i.e. the second zig-zag pattern).

It is admitted that the readout system of the applicants invention (i.e. Figure 5 of the present application) is different from the system disclosed in Mimura in view of Ochi, however as currently written claim 1 allows the alternate interpretation discussed above. If claim 1 were amended to read "characterized in that each row includes both said first and second light detecting elements alternately disposed and activated by first read lines to generate odd field signals, and in that said first and second light detecting elements in two adjacent rows disposed in a serrated manner are activated by second read lines to generate even field signals", and a similar amendment to claim 7 were made, the alternate interpretation would no longer be possible and claims 1 and 7 would be allowable over Mimura in view of Ochi.

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The applicant further argues that the sensor of Mimura is probably limited to a CCD implementation and not CMOS as in the subject of the present application. This is speculation and is irrelevant to the discussions of the claims since claim 1 (and its dependents) do not specifically require a CMOS image sensor. Applicant further argues that the offset of the resulting design of Mimura in view of Ochi results in a field offset of one pixel, instead of the one-half pixel offset of the present application. This is also irrelevant to the claim discussions as it is never claimed.

In regard to claims 2 and 6 the applicant argues that Ackland teaches the physical construction of a specific type of pixel using four transistors and that Ackland does not disclose how the specific type would be incorporated in the present invention. However Ackland teaches general advantages of using reset transistors (i.e. resetting the pixel) and source followers (i.e. buffering the pixel from output nodes) in imaging devices that could be used as teachings for incorporating similar structures in any imaging device, not just the specific type of device disclosed in Ackland.

In regard to claim 5, the applicant has not pointed out any claim language that would make claim 5 allowable over Ackland in view of Ochi, and as such the rejection of claim 5 stands.

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As the applicants arguments have been fully considered and are found to be non-persuasive, the rejections over Mimura in view of Ochi, Mimura in view of Ochi in further view of Ackland and Ackland in view of Ochi stand.

Claim Rejections - 35 USC § 103

- 5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mimura (US 6,249,643) in view of Ochi (US 4,542,409).

[claim 1]

In regard to claim 1, note that Mimura discloses an image sensor for sensing light of an image, said image sensor comprising a plurality of first (Figure 1, Item "n LINE") and second (Figure 1, Item "n+1 LINE") elements arranged in rows and columns for generating respective analog signals in proportion to the intensity of the light impinging respectively on each of the light detecting elements (Column 2, Line 64 – Column 3, Line 3), characterized in that the first and second light detecting elements in each row of the sensor are alternately disposed (Figure 2(b), the examiner notes that each row of first and each row of second elements are alternately disposed in a vertical direction) and in that the first and second light detecting elements in two adjacent rows are disposed in a serrated manner (Figure 2(b), the examiner notes that in two adjacent rows, n and n+1, the first and second elements are offset to form a serrated pattern). Therefore, it can be seen that Mimura lacks first read lines to generate odd field signals

and second read lines to generate even field signals, by selectively activating the first and second light detecting elements of the sensor.

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It is further noted that Mimura generates an interlaced readout by performing a "zigzag" readout of the array (Figure 5(a)), and changing the position of a switch (Figure 4. Item 78) to alter the output position of the current cell being read. Ochi suggests a simpler method for interlaced readout in which first and second read lines are used to read out even and odd field signals respectively (Figure 5, Items V_A and V_B), witch results in simplified interlaced readout (Column 6, Lines 10-25). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the readout line pattern of Ochi with the image sensor of Mimura to obtain an image sensor with is capable of simplified interlaced readout.

[claim 4]

In regard to claim 4, note that the first light detecting elements comprising two access transistors (Ochi, Figure 5, Items 73-1 and 73-2) coupled in parallel are activated by first (Ochi, Figure 5, Item 52) and second read (Ochi, Figure 5, Item 51) lines respectively, connected at the respective gates thereof, and wherein each of the second light detecting elements comprise two access transistors coupled in parallel and activated by the first read line (Ochi, Figure 5, Item 52) and another second read line (Ochi, Figure 5, Item 53), respectively, connected at the respective gates thereof.

[claim 7]

Claim 7 is a method claim corresponding to apparatus claim 1. Therefore, claim 7 is analyzed and rejected as previously discussed with respect to claim 1.

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7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mimura (US 6,249,643) in view of Ochi (US 4,542,40) as applied to claim 1 above, and further in view of Ackland et al. (US 5,576,763).

[claim 2]

In regard to claim 2, the interlaced readout image sensor of Mimura in view of Ochi comprises photocells which include a photodiode and two access transistors coupled in parallel (Ochi, Figure 5). Therefore, it can be seen that Mimura in view of Ochi lacks light detecting elements comprising a reset transistor and a source follower connected to the two parallel access transistors.

Ackland discloses an active pixel cell for use in an image sensor, which includes a reset transistor (Figure 3, Item 120; Column 4, Lines 19-22) to allow resetting of the cell and a source follower (Figure 3, Item 125; Column 4, Lines 31-34) to buffer the output of the cell. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the photo cell of Mimura in view of Ochi with the reset transistor and source follower of Ackland to include the benefits of resetting and buffering as taught by Ackland.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ackland et al. (US 5,576,763) in view of Ochi (US 4,452,409).

[claim 5]

In regard to claim 5, note that Ackland et al. discloses a light detecting element for use in a CMOS active pixel image sensor (Figure 1) comprising a translating means

comprising a reset transistor (Figure 1, Item 120) for resetting the initial state of a photodiode in the light detecting element (Column 4, Lines 19-22), a source follower (Figure 1, Item 125) for buffering an analog signal (Column 4, Lines 31-34) and a select or "access" transistor (Figure 1, Item 130; Column 4, Lines 36 and 37). Therefore, it can be seen that Ackland et al. lacks two access transistors coupled in parallel to each other and connected to the output of the source follower transistor.

Ochi teaches a solid state imager, which uses FET access transistors coupled in parallel to each other (Figure 5, Items 73-1 and 73-2; Column 5, Lines 35-52) in order for the pixel cell to be read-out by two separate read lines. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the single access transistor Ackland et al. with the two parallel access transistors of Ochi to allow the pixel cells of Ackland et al. to be able to be read-out by two separate read lines.

[claim 6]

In regard to claim 6, note that the parallel access transistors of Ochi (Figure 5, Items 73-1 and 73-2) are coupled in parallel and are activated by a first read line (Figure 5, Item 51) connected to the gate of the first access transistor and a second read line (Figure 4, Item 52) connected to the gate of the second access transistor as claimed.

Allowable Subject Matter

9. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims.

[claim 3]

In regard to claim 3, the prior art does not teach of fairly suggest a readout of light detecting elements in which the elements in two adjacent rows activated by second read lines substantially have average vertical location between the two adjacent rows and wherein the components of the first and second field signals are correlated with one another.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J Henn whose telephone number is (703) 305-8327. The examiner can normally be reached on M-F 7:30 AM - 5:00 PM, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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TJH 6/30/2004

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